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INTEGRATED CIRCUITS PROTECTED AGAINST REVERSE ENGINEERING AND METHOD FOR FABRICATING THE SAME USING VIAS WITHOUT METAL TERMINATIONS

by

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I. BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to the field of the prevention of reverse engineering of integrated circuits and/or making such reverse engineering so difficult and time-consuming as to make reverse engineering of integrated circuits non-feasible.

More particularly, this invention relates to using, in order to prevent and/or discourage such reverse engineering, vias (i.e., holes etched in the oxide layers between metal layers and then filled with metal to affect a connection between metal layers) either not beginning on a metal layer or not terminating on a metal layer.

2. Description of the Related Art.

The design and development of semiconductor integrated circuits require a thorough understanding of the complex structures and processes and involve many man-hours of work requiring high skill, costing considerable sums of money.

In order to avoid this time and effort, some developers resort to the practice of reverse engineering, disassembling existing devices manufactured by somebody else, and closely examining them to determine the physical structure of the integrated circuit, followed by slavishly copying the device. Thus, by obtaining a planar optical image of the circuits and by studying and copying them, typically required product development efforts are circumvented.

Such practices hurt the true developer of the product and impairs its competitiveness in the market-place, because the developer had to spend significant amounts of time and effort for the development, while the reverse engineer did not have to.

A number of approaches has been used in order to frustrate such reverse engineering attempts, particularly in the field of semiconductor integrated circuits.

For instance, U.S. Patent No. 5,866,933 to Baukus, et. al. teaches how transistors in complementary metal oxide-semiconductor (CMOS) circuit can be connected by implanted, hidden and buried lines between the transistors. This hiding is achieved by modifying the p+ and n+ source/drain masks. The implanted interconnections are further used to make a 3-input AND-circuit look substantially the same as a 3-input OR-circuit.

Furthermore, US Patents Nos. 5,783,846 to Baukus, et. al. and 5,930,663 to Baukus et. al. teach a further modification in the source/drain implant masks, so that the implanted connecting lines between transistors have a gap inserted, the length of which is approximately the length of the feature size of the CMOS technology being used. These gaps are called "channel blocks."

If the gap is "filled" with one kind of implant (depending on whether the implanted connecting line is "p" or "n"), the line conducts; if another kind of implant is used for the gap-filling, the line does not conduct. The reverse engineer must determine connectivity on the basis of resolving the "n" or "p" implant at the minimum feature size of the channel block. In addition, transistor sizes and metal connection routings are modified, in order to deprive the reverse engineer of using clues with which

he can find inputs, outputs, gate lines and so on as keys to the circuit functionality.

Practicing the inventions taught in the above-mentioned patents to secure an integrated circuit causes the reverse engineer to perform steps that are not always needed. These steps include: decomposing the circuit layer by layer, careful processing of each layer followed by imaging of the layer with exact registration to other layers, and having the required process to image and determine small area implants of specifically both - and p-types.

Once a particular standard circuit functionality has been determined, the reverse engineer will attempt to find some signature in the metal layers of that standard circuit which can exactly indicate the presence of that particular standard circuit in other places in the integrated circuit. If this can be done, that information can be entered into the reverse engineer's data base and automatic pattern recognition of the metal pattern is used to determine the circuit, without need for the extensive delayering. This would save considerable time and effort.

Therefore, there still exists a need for an inexpensive, easy-to-implement defensive method which can help to provide the enhanced protection against the reverse engineering of semiconductor integrated circuits, in particular to make such a signature impossible to determine. The present invention provides such a method.

II. SUMMARY OF THE INVENTION

This invention makes the use of vias to provide connections between metal layers unpredictable and difficult to be determined accurately. Hence, the circuit will appear to be one thing, while in fact it is something else. This is a good way to prevent reverse engineering.

Modern integrated circuits are constructed such that signals are routed between circuit/logic blocks (or sometimes between transistors within a single circuit/logic block) and input/output ports, via metallic lines. For purposes of compaction, more than one metal layer is used, the metal layers being separated by a deposited insulating layer, both metal layers being disposed on top of the semiconductor substrate. Connections between these metal lines are accomplished by using vias, for example, holes

etched in the insulating layer between metals. The vias are filled with a metal, typically, tungsten.

The gravamen of the present invention is to provide vias which either do not begin or do not terminate on a metal layer. Such non-metal terminating vias will look like an interconnection between adjacent metal layers/lines to the reverse engineer, but they in fact provide no such interconnection.

Such non-metal terminating vias will make it very difficult for a reverse engineer to determine what the signal routing pattern really is, making the process of reverse engineering more expensive and time consuming effectively rendering the circuit secure from such intrusion.

When the reverse engineer observes the top metal layer, dimples in the metal indicate the presence of vias. He will also observe the presence of the via after having removed the top metal layer. However, as a result of etching away the oxide layer between metal layers, down to the lower metal layer, the via is eliminated as well. Therefore, the reverse engineer is likely to assume that the metal layers are connected, because following the via to the lower level, where in fact it is not connected to the

lower metal layer, is difficult to accomplish.

The reverse engineer will have to assume the via connects with two metal lines, one in the upper metal layer and one in the lower metal layer, while in fact, the connection is only with, at most, one metal layer.

A first aspect of the invention provides a semiconducting device adapted to prevent and/or to thwart reverse engineering, including an insulating layer disposed on a semiconductor substrate, a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer and a via defined by said insulating layer, said via having a first end and a second end, wherein said first end of said via is connected to said first metal layer and said second end of said via terminates prior to reaching said second metal layer.

A second aspect of the invention provides a semiconducting device adapted to prevent and/or to thwart reverse engineering, including an insulating layer disposed on top of semiconductor substrate a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said

insulating layer, and a via defined by said insulating layer, said via having a first end and a second end, wherein said second end of said via is connected to said second metal layer and said first end of said via terminates prior to reaching said first metal layer.

A third aspect of the invention provides a method for preventing and/or thwarting reverse engineering, comprising steps of disposing an insulating layer on top of semiconductor substrate, forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer and forming a via defined by said insulating layer, said via having a first end and a second end, wherein said first end of said via is connected to said first metal layer and said second end of said via terminates prior to reaching said second metal layer.

A fourth aspect of the invention provides a method for preventing and/or thwarting reverse engineering, comprising steps of disposing an insulating layer on top of semiconductor substrate, forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer, and forming a via defined

by said insulating layer, said via having a first end and a second end, wherein said second end of said via is connected to said second metal layer and said first end of said via terminates prior to reaching said first metal layer.

III. BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where

FIG. 1 is a schematic diagram showing a typical via connecting two metal layers.

FIG. 2 is a schematic diagram showing how metal lines are located relative to one another.

FIG. 2(a) is a schematic diagram showing a via according to one embodiment of this invention, where the via does not terminate on a lower metal layer.

FIG. 2(b) is a schematic diagram showing a via according to another embodiment of this invention where the via does not

begin on an upper metal layer.

IV. DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows a usual via 1 connecting an upper metal layer 2 and a lower metal layer 3. The via 1 has two ends: a first end 1(a) and a second end 1(b). The upper and lower metal layers are separated by an insulating layer 4, typically made of silicon oxide. Insulating layers 5 and 6, typically, occur above and below metal layers 2 and 3. The insulating layers 4, 5 and 6 are disposed in a semiconductor device, preferably, an integrated circuit (not shown). The via 1 is filled with a metal, typically the same metal as the metal of metal layers 2 and 3, this metal usually being tungsten.

FIG. 2 shows that metal lines 2(a) and 3(a), within the two metal layers 2 and 3, respectively, do not typically run parallel. They are disposed in parallel planes, but the signal metal lines 2(a) and 3(a) are not parallel. Instead, the metal pattern, when viewed from the top, as shown on FIG. 2, is usually two arrays of lines proceeding in orthogonal directions, when viewed as projected onto a single plane. The metal lines 2(a) and 3(a) lie in different planes.

In order to confuse a rèverse engineer, two new structures shown on FIGs. 2(a) and 2(b) are offered, these structures comprising two embodiments of this invention.

FIG. 2(a) schematically depicts a structure, disposed on an integrated circuit (not shown) where the via 1 terminates on the upper metal layer 2, where the first end 1(a) is connected to the upper metal layer 2, but the second end 1(b) does not terminate on the lower metal layer 3. As seen on FIG. 2(a), the second end 1(b) is spaced from the conducting line made from the lower metal layer 3. A portion of insulating layer isolates the second end 1(b) from the lower metal layer 3.

In an alternative embodiment, shown on FIG. 2(b), also used on an integrated circuit (not shown) the via 1 terminates on the lower metal layer 3, but does not terminate on the upper metal layer 2. In this case, the second end 1(b) is connected to the lower metal layer 3, but the first end 1(a) is spaced from and thus isolated from the conducting line in the upper metal layer 2 by a portion of insulating layer.

The vias 1 of both embodiments are manufactured according to common methods of fabrication of vias known to those skilled in

the art. Usual design rule allowances, known to those skilled in the art, concerning the minimum spacing between an unterminated end of the via 1 and the metal layer 2 or 3, should be observed.

This invention can be used on any CMOS, bi-polar silicon, or group III-V integrated circuit. The references herein have been with regard to two metal layers. However, a device may have many metal layers and this invention can be used to imply a connection, but not a connect, between any two of many metal layers.

This invention is a circuit trick technique. It can be used together with other techniques disclosed in the previously discussed prior art to prevent reverse engineering. The composite of such previously known techniques is to make the connections between transistors difficult to determine. The reverse engineer will have to carefully analyze each CMOS transistor pair rather that utilize automatic circuit and pattern recognition techniques.

As a part of his or her above-mentioned analysis of each CMOS transistor pair, a reverse engineer is likely to look carefully at the metal traces and via 1 carefully removing one metal layer,

determining the location of vias to the layer beneath to see the connection. When viewing the top metal layer 2, the reverse engineer looks for dimples in the top metal surface. These dimples indicate the presence of a via 1 beneath them, and this via 1 ordinarily connects to a metal layer below.

Seeing the dimple, the reverse engineer will, therefore, assume that underneath the dimple there is a via connecting to the metal layer below. He will proceed by checking the correctness of his or her assumption by etching away the top metal layer and noting the via 1 beneath. However, when etching away the via metal, along with the insulating layer 4 surrounding it, it is very difficult for the reverse engineer to determine if the via 1 does indeed terminate on the metal layer below.

By beginning or terminating a via 1 where there is no metal present, this invention will make the reverse engineer's task very difficult. He will assume all sorts of connections where there are none. Should he or she discover his or her error, he or she will have to use cross-sectioning of the circuit to determine where the missing metal portions are and this process is prohibitively expensive and labor-extensive, effectively making the circuit much more secure.

The structures of this invention can be easily inserted into an integrated circuit fabrication process according to techniques known to those skilled in the art. No additional processing steps are needed.

Having described the invention in connection with several embodiments thereof, modification will now suggest itself to those skilled in the art. As such, the invention is not to be limited to the described embodiments except as required by the appended claims.